whereby said preferred Manhattan direction conductors of said self contained layer within said first metal group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said self contained layout conductors are deposed in either a horizontal or vertical direction.

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REMARKS

This Amendment is concurrently filed with the filing of a Request for Continued Examination.

In the Final Office Action dated September 25, 2002, claims 16-23, 26, 28-35 and 38 were rejected under 35 USC 103(e), as being unpatentable over US Patent 5,723,908, issued to Fuchida et al. (hereafter referred to as *Fuchida et al.*), in view of US Patent 6,448,591, issued to Juengling (hereafter referred to as *Juengling*). Claims 24 and 36 are rejected under 35 USC 103(a) as being unpatentable over *Fuchida et al.*, and *Juengling*, in further view of US Patent 5,635,736, issued to Funaki et al., (hereafter referred to as "*Funaki et al.*"). Finally, claims 25, 27, 37 and 39 were rejected under 35 USC 103(a) as being unpatentable over *Fuchida et al.*, and *Juengling*, in further view of US Patent 6,262,487, issued to Igarashi et al. (hereafter referred to as *Igarashi et al.*)

Claims 16-25, 27-37 and 39 are currently pending in this application.

Overview of the Claimed Invention:

An integrated circuit employs diagonal wiring geometries to provide noise immunity from self contained layout sections. A self contained layout section, or pre-configured or pre-designed blocks, includes conductors that are routed independent from other circuits in the integrated circuit. The self contained layout section, which implement Manhattan wiring geometries, may utilize one or more wiring (*e.g.*, metal layers) of the integrated circuit. Diagonal wires are routed over the self contained layout section. The self contained layout section is not affected by the diagonal wires deposed on metal layers above them. The self contained layout section may incorporate memory circuits, small cells that implement simple logic functions, as well as large functional blocks that implement specific functionalities.

A. The Cited References Do Not Disclose A Self Contained Layout Section With Conductors Routed Independent From Conductors In An Adjacent Second Metal Layer Group.

Amended claims 16 and 28 recite:

said self contained layout section comprising a routing of conductors developed independent from routing of conductors for circuits outside said self contained layout section in said integrated circuit;

...

wherein conductors for said second metal layer group are routed independent from routing of conductors for said self contained layout section.

As claimed, the "self contained layout" of the present invention comprises "a routing of conductors developed independent from routing of conductors for circuits outside said self contained layout section."

The Specification discloses examples of "self contained layout sections" (*e.g.*, IP blocks) with metal layers of diagonal wiring deposed above the IP blocks.

> Figure 11 is an example of using diagonal wiring in metal layers disposed above IP blocks. For this example, an integrated circuit 1100 includes pre-configured or IP blocks 1110, 1120 and 1130. The IP blocks 1110, 1120 and 1130 are self-contained within layers "1", "2" and "3" of integrated circuit 1100. (Specification, page 22, lines 10-13).

The Examiner cites *Fuchida et al.* for disclosing the claimed "first metal layer group" and "second metal layer group." In the cited section, *Fuchida et al* disclose a five layer wiring structure with a first signal line layer, a second signal layer, a first power/ground line layer, located beneath the layer 10, a second power/ground layer 40 located above the layer 30, and a third power/ground layer 50 located between the layers 10 and 30. For the fifth embodiment, the strips of the first signal line layer 10 extend at 90 degrees to those of the second signal line layer 30 in a skewed position. The strips of the power/ground line layers 20, 40 and 50 extend at 45 degrees to strips of both signal line layers 10 and 30 in a skewed position. Figure 11 of *Fuchida et al.* shows the fifth embodiment.

The Examiner states that *Fuchida et al.* do not disclose a self-contained layout section of the first metal layer group comprising conductors deposed in a preferred Manhattan direction. However, the Examiner contends that *Juengling* discloses, in Figure 1, a self-contained layout section Z of the first metal layer group comprising conductors deposed in a preferred Manhattan direction (2L). With regard to the Z region, *Juengling* discloses an "arbitrary region" to have a substantially rectangular shape that includes parallel vertical boundaries and parallel horizontal boundaries. *Juengling* disclose the Z region as an arbitrary region, and as such, does not disclose that the Z region comprises "a routing of conductors developed independent from routing of conductors for circuits outside said self contained layout section." Accordingly, because *Juengling* does not teach or suggest a "self contained layout" with "a routing of conductors developed independent from routing of conductors for circuits outside said self contained layout section", *Juengling* does not render the claimed invention unpatentable.

B. The Conductors Of The Second Metal Layer Group Do Not Electrically Interfere With Conductors Of The Self Contained Layout Section.

The Examiner concluded that it would be obvious to one of ordinary skill in the art at the time the invention was made to modify *Fuchida et al.* by using a preferred Manhattan direction as taught by *Juengling*. The Examiner reasoned that an ordinary artisan would have been motivated to modify in a manner described above for at least the

purpose of providing isolated lines. However, the purpose of the present invention, as claimed, is not to "provide isolated lines." Instead, the purpose is to permit placement on an integrated circuit a self-contained layout section in any manner (allowing either horizontal or vertical conductors) such that horizontal or vertical conductors of the self-contained layout within the first metal layer group do not electrically cross couple with conductors of the second metal layer group. Accordingly, because the cited references do not disclose or teach placing a "self-contained layout section", as claimed, on a metal layer directly adjacent to a second metal layer group with diagonal wires, the cited references do not render the claimed invention unpatentable.

The ability to place a self contained layout directly adjacent another metal layer that routes conductors is substantial. Amended claims 16 and 28 set forth this substantial benefit. Specifically, amended claims 16 and 28 recite:

whereby said preferred Manhattan direction conductors of said self contained layer within said first metal group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said self contained layout conductors are deposed in either a horizontal or vertical direction.

The Specification discusses this advantage of the claimed invention. Specifically, with regard to electrical cross-coupling, the Specification of the present application discloses:

> In a hierarchical design approach, wires in a subsection of the IC are routed independent of other areas of the IC. For example, an IP block, with Manhattan directional wires routed independent of other portions of the IC, may be integrated into an IC employing diagonal wires without noise coupling concerns. (Specification, page 22, lines 5-9).

The Specification further discloses:

> Since the IP blocks utilize Manhattan wiring geometries, the use of diagonal wires in metal layers above the IP blocks do not result in noise coupling between the wires on the metal layer(s) and the wires on the IP block. (Specification, page 22, lines 3-5).

An example of the claimed invention is illustrated in Figure 11 of the Specification. This example illustrates how the claimed invention permits routing diagonal conductors directly above self contained layout sections (*e.g.*, IP blocks).

> Figure 11 shows a top view of a wiring layer above layer three (*i.e.*, layer "4" or above). As shown in Figure 11, the use of diagonal wiring permits routing diagonal wires above IP blocks 1110, 1120 and 1130. Because the preferred wiring direction in this metal layer is not either horizontal or vertical, electrical emanations from the diagonal wires do not directly coupled to the wire layers in the IP blocks, and thus do not cause a degradation in circuit performance. (Specification, page 22, lines 14-19).

Using the claimed invention, the orientation of the self contained layout in the integrated circuit is immaterial. For example, if the self contained layout is oriented such that the Manhattan conductors are deposed in a vertical position, then the diagonal directional wires of the second metal layer group do not electrically interfere. Similarly, if the self contained layout is oriented such that the Manhattan conductors are situated in a horizontal position, then the diagonal directional wires of the second metal layer group do not electrically interfere with the conductors of the first metal layer group.

Accordingly, Applicants respectfully contend that the cited references, either alone or in combination, do not disclose or suggest the benefit of using diagonal wiring in a metal layer adjacent to a self contained layer, as claimed. Thus, for this additional reason, the claimed invention is patentable over the cited references.

Dependent Claims:

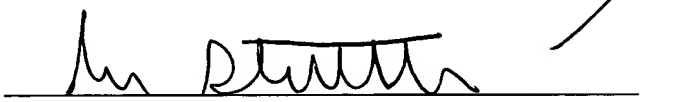
Dependent claims 17-25 and 27 are depend, either directly or indirectly, upon independent claim 16, and therefore for the same reasons claim 16 is patentable over the cited references, claims 17-25 and 27 are also patentable over the references. Similarly, claims 29-37 and 39 are directly or indirectly, dependent, upon claim 28, and therefore for the same reasons claim 28 is patentable over the cited references, claims 29-37 and 39 are also patentable over the references.

CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

STATTLER JOHANSEN & ADELI LLP



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The Amended Claims

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

16. (Twice Amended) An integrated circuit comprising:

a plurality of metal layers comprising a plurality of conductors to interconnect components in an integrated circuit, said metal layers comprising:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors, and said self contained layout section comprising a routing of conductors[, for a portion of said metal layer,] developed independent from routing of conductors for circuits outside said self contained layout section in said integrated circuit; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout section, and wherein conductors

for said second metal layer group are routed independent from routing of conductors for said self contained layout section,

whereby said preferred Manhattan direction conductors of said self contained layer within said first metal group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said self contained layout conductors are deposed in either a horizontal or vertical direction.

28. (Twice Amended) A method for deposing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors and said self contained layout section comprising a routing of conductors[, for a portion of said metal layer,] developed independent from routing of conductors for circuits outside said self contained layout section in said integrated circuit; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent

to said portion of said metal layer for said self contained layout, and wherein conductors for said second metal layer group are routed independent from routing of conductors for said self contained layout section,

whereby said preferred Manhattan direction conductors of said self contained layer within said first metal group do not electrically cross-couple with conductors of said second metal layer group regardless of whether said self contained layout conductors are deposed in either a horizontal or vertical direction.